

VERILOG DESIGN OF INPUT/OUTPUT PROCESSOR
WITH BUILT-IN-SELF-TEST

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*Specially dedicated to my beloved parents, younger brother, supervisor, lectures,
fellow friends and those who have guided and inspired me throughout my journey of
education.*

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ABSTRACT

This project has a final goal of designing an I/O processor (IOP) with embedded built-in-self-test (BIST) capability. The IOP core design was originally design in VHDL modeling has been migrated to Verilog HDL modeling in this project. BIST is one of the most popular test technique used nowadays. The embedded BIST capability in IOP designed in this project has the objectives to satisfy specified testability requirements and to generate the lowest-cost with the highest performance implementation. Linear Feedback Shift Register (LFSR) is used to replace the expensive testers to generate pseudo random test pattern to IOP while Multiple Input Signature Register (MISR) is able to compact the IOP output response into a manageable signature size. In this project, the designed is coded in Verilog hardware description language at register transfer level (RTL), synthesized using Altera Quartus II using FPFA device from APEC20KE family, RTL level compilation and simulation using Modelsim v6.1b and gate level timing simulation using Modelsim-Altera v6.1g. This project was scheduled for two semester in which the activities to study and determine hardware specifications, requirements, functionalities and Verilog HDL migration were done in first semester whereas activities to design, synthesis, compile, simulate, and validate were carried out in semester 2. IOP with BIST capability contributes additional 30% hardware overhead but is somehow reasonable considering the test performance obtained and the ability of the BIST block provides high fault coverage.

ABSTRAK

Projek ini bertujuan untuk merekapi satu pemproses masukan/keluaran (IOP) dengan keupayaan terbina dalam uji sendiri (BIST). Pada asalnya, IOP dimodel dalam bahasa VHDL telah ditukar kepada rekapi dalam bahasa Verilog HDL. BIST merupakan salah satu teknik yang paling banyak diguna hari ini. Keupayaan BIST yang dimasukkan ke dalam IOP bertujuan untuk memenuhi keperluan keujian tertentu dan menjana kos yang paling rendah dengan prestasi yang paling tinggi. Pendaftar Anjakan Suap Balik Linear (LFSR) diguna untuk menggantikan penguji yang mahal and untuk menjana ujian yang pseudo rawak kepada IOP. Padahal, Pendaftar Tandatangan Pelbagai Masukan (MISR) boleh diguna untuk mengurangkan keluaran sambutan dalam untuk tandatangan yang boleh mengurus. Dalam projek ini, IOP dimodel dalam bahasa Verilog dalam tahap pendaftar pindah (RTL), sistesis dengan menggunakan Altera Quartus II dengan FPGA dari keluarga APEC20KE, kompil rekapi dalam tahap RTL, simulasi rekapi dengan menggunakan Modelsim v6.1b dan simulasi tahap get dengan Modelsim-Altera v6.1g. Project ini dirancang bagi 2 semester dengan aktiviti untuk menentukan spesifikasi rekapi, keperluan dan fungsi rekapi and ketukaran kepada IOP dalam bahasa Verilog dilaksanakan semasa semester 1, manakala aktiviti rekapi, sistesis, kompil dan simulasi dilaksanakan dalam semester 2. IOP dengan keupayaan BIST terbina dalam menbesarkan IOP sebanyak 30%, tetapi dianggap boleh tahan and boleh diterima memandangkan prestasi uji yang cemerlang and keupayaan BIST untuk memberi liputan kesalahan yang begitu tinggi.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	xi
	LIST OF FIGURES	xii
	LIST OF ABBREVIATIONS	xv
	LIST OF APPENDICES	xvi
CHAPTER 1	INTRODUCTION	
1.1	Overview and Problem Statement	1
1.2	Objectives	3
1.3	Scope of Work	4
1.4	Project Contributions	5
1.5	Thesis Outline	6

CHAPTER 2 BACKGROUND AND THEORY

2.1	An Overview of Serial Communication	7
2.2	UART	8
2.3	BIST – An Overview	10
2.3.1	BIST Process	10
2.3.2	BIST Implementation	11
2.3.3	BIST Pattern Generation	13
2.3.3.1	Standard LFSR	14
2.3.4	BIST Response Compaction	16
2.3.5	Built-In Logic Block Observers	18

CHAPTER 3 METHODOLOGY AND DESIGN TOOLS

3.1	Project Design and Implementation Flow	22
3.2	Verilog HDL	28
3.3	Mentor Graphics Modelsim v6.1	29
3.4	FPGA Synthesis	31
3.5	Altera Quartus II 6.1	32
3.6	Modelsim-Altera v6.1g Web Edition	34

CHAPTER 4 I/O PROCESSOR CORE DESIGN

4.1	IOP – An Overview	36
4.2	IOP Architecture	38
4.3	Message Format	41
4.4	IOP Operation	43

CHAPTER 5 DESIGN OF IOP WITH EMBEDDED BIST CAPABILITY

5.1	Top Level Architecture	44
5.2	BIST Module	51
5.2.1	BIST DPU Module	54
5.2.1.1	<i>Command Select Mux</i>	57
5.2.1.2	<i>Functional Block</i>	58
5.2.1.3	BILBO	60
5.2.1.4	<i>Decoder Block</i>	65
5.2.1.5	<i>Command Decoder</i>	67
5.2.1.6	<i>NextCmd Select</i>	68
5.2.2	BIST CU Module	69
5.3	IOP BIST Operation	83

CHAPTER 6 SIMULATION, VERIFICATION AND RESULTS ANALYSIS

6.1	Verilog HDL Code Efficiency Gain	90
6.2	Design Compilation, Synthesis and Timing Analysis	92
6.2.1	Design Synthesis and Analysis	92
6.2.2	Fitter and Assembler	94
6.2.3	Design Timing Analysis	95
6.3	Design Test bench	98
6.4	IOP Simulations and Discussion	100
6.4.1	Functional Mode	100
6.4.2	BIST Mode	108
6.4.2.1	Fault Free Circuit Simulation	109
6.4.2.2	Faulty Circuit Simulation	113

CHAPTER 7 CONCLUSION AND FUTURE WORK

7.1	Conclusion	116
7.2	Recommendation for Future Works	117

LIST OF REFERENCES	120
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APENDIX A-B	122-192
--------------------	----------------

LIST OF TABLES

TABLE NO	TITLE	PAGE
Table 2.1	Control modes for the BILBO of figure 2.6	19
Table 4.1 (a)	Table of Control Bytes	41
Table 4.1 (b)	Table of Command Bytes	42
Table 5.1	BIST module Input, Output and Internal signal	53
Table 5.2	BIST DPU Input, Output signal	56
Table 5.3	<i>Command Select Mux</i> output table	58
Table 5.4	BILBO block in BIST DPU operation mode	60
Table 5.5	Input and output signals for BIST CU module	70
Table 5.6	BIST CU RTL control sequences table	82
Table 6.1	Verilog HDL migration code efficiency gain	91
Table 6.2	Analysis and Synthesis - IOP Resource Usage Summary	94
Table 6.3	Summary of IOP timing analysis	96

LIST OF FIGURES

FIGURE NO	TITLE	PAGE
Figure 2.1	UART data frames format	9
Figure 2.2	BIST hierarchy	11
Figure 2.3	BIST architecture	12
Figure 2.4	Standard n-stage LFSR circuit	14
Figure 2.5	Multiple input signature register	18
Figure 2.6	BILBO circuit	19
Figure 2.7	BILBO in serial scan mode	19
Figure 2.8	BILBO in LFSR mode	20
Figure 2.9	BILBO in normal D flip-flop mode	20
Figure 2.10	BILBO in MISR mode	21
Figure 3.1	Project design flow	23
Figure 3.2	Multiple abstractions for digital system design	24
Figure 3.3	Digital design flow	25
Figure 3.4	Project design and implementation flow	27
Figure 3.5	General structure of an FPGA	31
Figure 3.6	Quartus II design flow	33
Figure 4.1	Overall System Architecture of PC-based Design and Test System for digital design in FPGA	37
Figure 4.2	IOP Architecture	40
Figure 4.3	Data Packet Format	41
Figure 5.1	IOP block diagram with embedded BIST	45

Figure 5.2	IOP design with embedded BIST capability architecture	46
Figure 5.3	IOP with embedded BIST Design Hierarchy	47
Figure 5.4	High level BIST operation flow	48
Figure 5.5	BIST module block diagram	52
Figure 5.6	BIST DPU module block diagram	55
Figure 5.7	<i>Command Select Mux</i> block diagram	57
Figure 5.8	<i>Functional Block</i> diagram	59
Figure 5.9	BILBO circuit	61
Figure 5.10	BILBO LFSR block diagram	62
Figure 5.11	BILBO LFSR mode operation waveform	62
Figure 5.12	BILBO scan mode operation waveform	63
Figure 5.13	BILBO D flip-flop mode operation waveform	63
Figure 5.14	BILBO MISR block diagram	64
Figure 5.15	BILBO D MISR mode operation waveform	65
Figure 5.16	<i>Decoder Block</i> diagram	66
Figure 5.17	<i>Command Decoder</i> block diagram	68
Figure 5.18	<i>NextCmd Select</i> block diagram	68
Figure 5.19	BIST CU block diagram	69
Figure 5.20	BIST CU RTL Code	71
Figure 5.21	IOP BIST operation flow chart	84
Figure 6.1	Full compilation of the design by Quartus II	97
Figure 6.2	Design test bench	99
Figure 6.3	Waveform for functional mode simulation 1 result	101
Figure 6.4	Waveform for functional mode simulation 2 result	103
Figure 6.5	Waveform for functional mode simulation 3 result	105
Figure 6.6	Waveform for functional mode simulation 4 result	106
Figure 6.7	Waveform for functional mode simulation 5 result	108
Figure 6.8	Simulation waveform 1 for fault free IOP in BIST mode	110
Figure 6.9	Simulation waveform 2 for fault free IOP in BIST mode	112

Figure 6.10	Simulation waveform 3 for fault free IOP in BIST mode	113
Figure 6.11	Simulation waveform 1 for faulty IOP in BIST mode	114
Figure 6.12	Simulation waveform 2 for faulty IOP in BIST mode	115

LIST OF ABBREVIATIONS

ASIC	-	Applications Specific Integrated Circuit
ATPG	-	Automatic Test-Pattern Generation
BILBO	-	Built-In Logic Block Observers
BIST	-	Built-In-Self-Test
CAD	-	Computer Aided Design
CU	-	Control Unit
CUT	-	Circuit Under Test
DPU	-	Data Path Unit
DUT	-	Design Under Test
FES	-	Front End Subsystem
FPGA	-	Field Programmable Gate Array
HDL	-	Hardware Description Language
IC	-	Integrated Circuit
IP	-	intellectual property
LFSR	-	Linear Feedback Shift Register
LSB	-	Least Significant Bit
MISR	-	Multiple Input Signature Register
I/O	-	Input/Output
PC	-	Personal Computer
ROM	-	Read-Only-Memory
RTL	-	Register Transfer Level
UART	-	Universal Asynchronous Receiver/Transmitter
SDF	-	Standard Delay Format
XOR	-	Exclusive OR

LIST OF APPENDIXS

APPENDIX	TITLE	PAGE
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APPENDIX A - Module Block Diagram and Verilog HDL Code

A1	Block diagram and VHDL code for <i>Testbench</i> module	122
A2	Block diagram and Verilog HDL code for <i>IOP</i> module	126
A3	Block diagram and Verilog HDL code for <i>clk_1mhz</i> module	128
A4	Block diagram and Verilog HDL code for <i>bist</i> module	129
A5	Block diagram and Verilog HDL code for <i>bis_cu</i> module	131
A6	Block diagram and Verilog HDL code for <i>bis_dpu</i> module	139
A7	Block diagram and Verilog HDL code for <i>bilbo</i> module	146
A8	Block diagram and Verilog HDL code for <i>DFFlop</i> module	148
A9	Block diagram and Verilog HDL code for <i>IOP_CU</i> module	148
A10	Block diagram and Verilog HDL code for <i>IOP_DPU</i> module	158
A11	Block diagram and Verilog HDL code for <i>IO_Interface</i> module	159
A12	Verilog HDL code for <i>Interface</i> module	160
A13	Block diagram and Verilog HDL code for <i>Buffers</i> module	161
A14	Verilog HDL code for <i>Register</i> module	163
A15	Verilog HDL code for <i>T_output_reg</i> module	164
A16	Block diagram and Verilog HDL code for <i>Input_card</i> module	164
A17	Verilog HDL code for <i>Trans_comparator</i> module	166

A18	Verilog HDL code for <i>Counter</i> module	167
A19	Block diagram and Verilog HDL code for <i>Output_card</i> module	167
A20	Verilog HDL code for <i>Poll_comparator</i> module	169
A21	Block diagram and Verilog HDL code for <i>UART</i> module	170
A22	Block diagram and Verilog HDL code for <i>C_transmit</i> module	170
A23	Block diagram and Verilog HDL code for <i>C_receive</i> module	173
A24	Block diagram and Verilog HDL code for <i>Status_reg</i> module	175
A25	Block diagram and Verilog HDL code for <i>UART_Comm</i> module	176
A26	Verilog HDL code for <i>Clock_generator</i> module	177
A27	Block diagram and Verilog HDL code for <i>UART_Receiver</i> module	178
A28	Verilog HDL code for <i>Receiver_CU</i> module	179
A29	Block diagram and Verilog HDL code for <i>Receiver_DPU</i> module	182
A30	Verilog HDL code for <i>Bit_counter1</i> module	183
A31	Verilog HDL code for <i>Rcv_shftreg</i> module	183
A32	Verilog HDL code for <i>Sample_counter</i> module	184
A33	Block diagram and Verilog HDL code for <i>UART_Transmitter</i> module	184
A34	Block diagram and Verilog HDL code for <i>Transmitter_CU</i> module	185
A35	Block diagram and Verilog HDL code for <i>Transmitter_DPU</i> module	187
A36	Verilog HDL code for <i>Datareg</i> module	188
A37	Verilog HDL code for <i>Bit_counter</i> module	189
A38	Verilog HDL code for <i>Shftreg</i> module	190

APPENDIX B

B1	VHDL to Verilog HDL Conversion Table	191
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CHAPTER 1

INTRODUCTION

This chapter gives an overview of the whole project, starts with the project background and problem statement, followed by the project objectives, scopes, project contributions and thesis outline

1.1 Overview and Problem Statement

The UTM PC-based FPGA Prototyping System consists of the I/O Processor (IOP) core and the Front-End Subsystem. Please refer to thesis titled “*PC-Based FPGA Prototyping System – Front-End Subsystem Design*” (2005) by Ng, Shuh Jiuan and “*PC-Based FPGA Prototyping System – I/O Processor Design*” (2005) by Chua, Lee Ping for more detail of the system design. The system is designed to enable users to send input data to Design-Under-Test (DUT) and obtains the DUT outputs displays on the Personnel Computer (PC) screen. This project will focus on discussing the IOP with embedded Built-In-Self-Test capability design.

IOP is a soft core that can be used to handle data communication between the PC and DUT in the FPGA-based Prototyping Board. The UART module in IOP is a soft core that used to conduct serial I/O communication. A universal asynchronous receiver/transmitter (UART) is a type of asynchronous receiver/transmitter computer hardware which is used to translate data between parallel and serial interfaces. It is commonly used for serial data telecommunication. A UART converts bytes of data to and from asynchronous start-stop bit streams represented as binary electrical impulses. It is mainly used at broadband modem, base station, cell phone, and PDA designs

It is crucial that the IOP is functioning correctly and is fault free in real silicon or FPGA board to ensure that the data sends to the DUT inputs are correct and outputs from the DUT send back to the Front End Subsystem is reliable.

With the increasing growth of sub-micron technology has resulted in the difficulty of testing. Manufacturing processes are extremely complex, making the manufacturers to consider testability as a requirement to assure the reliability and the functionality of each of their designed circuits. Built-In-Self-Test (BIST) is one of the most popular test technique used. For design and test development, BIST significantly reduces the costs of automatic test-pattern generation (ATPG) and also reduces the likelihood of disastrous product introduction delays because of a fully designed system cannot be tested.

A Universal Asynchronous Receive/Transmit with BIST capability has the objectives of firstly to satisfy specified testability requirements, and secondly to generate the lowest-cost with the highest performance implementation. Although BIST slightly increases the cost because of the BIST hardware overhead in the design and test development, due to added time required to design and added pattern generators, response compactors, and testability hardware. However, it is normally less costly than test development with ATPG.

With the reasons discussed above, this project focuses on the design of the embedded BIST architecture for an IOP. The designs will be implemented using Verilog Hardware Description Language (HDL) at the Register Transfer Level (RTL) abstraction level. BIST technique will be incorporated into the IOP design before the overall design is synthesized by means of reconfiguring the existing design to match testability requirements.

1.2 Objectives

The main objective of this project is to design a serial I/O Processor (IOP) logic core with the Built-in-Self-Test (BIST) capability using Verilog HDL.

This entails the following sub-objectives:

1. To migrate the UTM serial I/O processor (IOP) from VHDL to Verilog HDL modeling.
2. To upgrade the I/O Processor with Built-In-Self-Test capability.
3. To explore the possibility for implementation of the I/O module design with Altera APEX20 family Field Programmable Gate Array (FPGA).

1.3 Scopes of Work

- (a) IOP was originally design in using VHDL. It is converted to Verilog HDL design.
- (b) IOP is upgraded with embedded BIST capability.
- (c) The design is modeled in Verilog HDL at the RTL abstraction level.
- (d) This project is limit to design, simulate, validate and verify the design at RTL level using Mentor Graphic's Modelsim v6.1 b.
- (e) In this project, the design is synthesized into gate level netlist with Altera EP20K200EFC484-2X FPGA board using Altera's Quartus II 6.1.
- (f) Gate level timing simulation, validation and verification will be performed using Modelsim-Altera 6.1g.
- (g) The design is targeting based on opportunistic to implement into Altera's EP20K200EFC484-2X FPGA board.

1.4 Project Contributions

The IOP is migrated to Verilog HDL which contributes several advantages. Verilog HDL allows different levels of abstraction to be mixed in the same models and thus can define a hardware model in terms of switches, gates, RTL, or behavioral code. Besides, most popular logic synthesis tools support Verilog HDL. This makes it the language of choice for many ASIC companies. More important, all fabrication vendors provide Verilog HDL libraries for post logic synthesis simulation. Thus, designing a chip in Verilog HDL allows the widest choice of vendors. On top of that, compared to VHDL, Verilog HDL provides better code efficiency and easier to learn. Nowadays, most IC design company like Intel, Altera, Avago and other companies have migrated HDL design from VHDL to Verilog.

BIST is getting more and more important today. New ASIC (Applications Specific Integrated Circuit) designs nowadays are having embedded BIST. An IOP with BIST capability helps UTM Faculty of Electrical (FKE) in future research of the area of IC testing. This project also serves as a starting point and proof of concept. It can be a soft core IP (intellectual property) for UTM FKE and helps FKE to own its own IC design with BIST.

With the implementation of BIST, it enables to test IOP automatically through the self-generated test with exhaustive data values. This ensures the IOP chip is fault free by having very high fault coverage testing. With embedded BIST, expensive tester requirements and testing procedures starting from circuit or logic level to field level testing are minimized and this reduces the chip or system test cost. The reduction of the test cost will lead to the reduction of overall production cost.

IOP with BIST capability at the same time ensures the fault free circuit and thus making sure that the input data from Front End Subsystem through the IOP to DUT are correct as well as the DUT outputs values are reliable.

1.5 Thesis Outline

This thesis concentrates on the theory and design of IOP with embedded BIST capability and its functionality. This thesis is organized into 7 chapters. Chapter 1 is an overview of the project, objectives, project scope, project contributions and thesis outline. Chapter 2 discusses the project background, literature survey and theory which includes theory of serial communication, the UART and the overview of Built-In-Self-Test such as the BIST process, implementation, architecture and design

Chapter 3 elaborates the project methodology and the CAD design tools. It discusses the project design and implementation flow and CAD tools used in working out this project. Chapter 4 is the gives an overview of the UTM IOP design. This chapter includes the architecture of the IOP, messages format and IOP operations.

Chapter 5 describes core chapter of this thesis, which will describe in more detail the BIST module design includes the BIST architecture, operations, control unit as well as data path unit (DPU). Chapter 6 elaborates the simulation, results and analysis of IOP with embedded BIST capability. Finally, Chapter 7 concludes this project with conclusion, project limitations, recommendations and suggested future works.

LIST OF REFERENCES

1. Stephen Brown, Zvonko Vranesic. *Fundamentals Of Digital Logic With VHDL Design*. International Edition. Singapore. McGraw-Hill. 2000
2. Chua Lee Ping. *PC-BASED FPGA PROTOTYPING SYSTEM – I/O PROCESSOR DESIGN*. Thesis Universiti Teknologi Malaysia. 2005
3. Ng Shu Jiuan. *PC BASED FPGA PROTOTYPING SYSTEM – DESIGN OF FRONT END SUBSYSTEM*. Thesis Universiti Teknologi Malaysia. 2005
4. Frank Durda. “Serial and UART Tutorial”. (*Internet source*) 1996
5. Mohd Yamani Idna Idris, Mashkuri Yaacob, Zaidi Razak . *A VHDL IMPLEMENTATION OF UART DESIGN WITH BIST CAPABILITY*
Faculty of Computer Science and Information Technology. University of Malaya
6. Michael L. Bushnell. *Essential of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuit* . Springer
7. John D. Carpinelli. *Computer Systems Organization & Architecture*. International Edition, Pearson Education.
8. John P. Hayes. *Computer Architecture and Organization*. International Edition, McGraw-Hill.

9. IEEE Standard 1364-2001 Verilog Hardware Description Language Reference Manual
10. Modelsim v6.1b User Reference Manual. (*Internet source*)
11. Introduction To Quartus II Manual. (*Internet source*)